XV

501.18758C14

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

K. SHIMOHIGASHI et al.

Serial No.:

Not Yet Assigned

Filed:

May 23, 1995

For:

SEMICONDUCTOR MEMORY

Group:

2511

Examiner:

T. Fears

PRELIMINARY AMENDMENT

Honorable Commissioner of Patents and Trademarks Washington, D.C. 20231 May 23, 1995

sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 1-19 without prejudice or disclaimer.

Please add the following new claims:



-> 20. A semiconductor memory comprising:

a pair of data lines which are formed substantially in parallel to each other;

